0.25-μm BiCMOS Receivers for Normal and Micro GSM900 and DCS1800 Base Stations

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***Abstract*—This paper describes two integrated RF receivers with low noise and high linearity for GSM900 and DCS1800 base stations. The chips were fabricated using a 0.25-μm BiCMOS process. This is the first silicon-integrated radio front-end that can be used to meet global system for mobile communications normal and micro base-station specifications reported to date. Noise figure, gain, and output infrared third-order intercept point are 2.1 dB, 25.8 dB, and 25.7 dBm for GSM900 and 3.3 dB, 21.3 dB, and 22.5 dBm for DCS1800, respectively.**

***Index Terms*—Base station, BiCMOS integrated circuits, DCS1800, GSM900, receiver.**

I. Introduction

THE design of a receiver front-end for cellular base stations is more challenging than for handsets due to the stringent requirements set by the global system for mobile communications (GSM) specifications [1] on receiver reference sensitivity and intermodulation and blocking characteristics. Unlike the handset that handles only one channel at a time, a base-station receiver handles multiple channels and cannot use gain control to increase its dynamic range. While the radio front-ends in handsets can be integrated in low-cost silicon technologies, the base-station radio front-end currently uses expensive components in GaAs technologies. Even a few reported efforts toward a higher integration level still use GaAs technologies [2], [3]. After a study of both system requirements [1] and integrated-circuit (IC) technology constraints, we found that it is feasible to realize a base-station RF integrated circuit (RFIC) front-end in low-cost silicon technologies by choosing the appropriate radio architecture and specification partitioning within the receiver chain. The low phase-noise voltage-controlled oscillator (VCO) in [4] is an example.

This paper presents base-station RFIC receivers for both GSM900 and DCS1800 systems and demonstrates that both receiver chips, with external image filtering, meet the sensitivity and linearity requirements for GSM900 and DCS1800 "normal" and "micro" base stations, as defined in [1]. This is illustrated by using an example receiver chain in each band. The chips presented here achieve low noise figure (NF) and high infrared third-order intercept point (IP3) simultaneously without any gain control. The chips were fabricated using a 0.25-μm BiCMOS process on a silicon substrate of resistivity 10 $\Omega \cdot$ cm. All the inductors that the receiver chips require are integrated on-chip. The NF, gain, and output IP3 for GSM900 are 2.1 dB, 25.8 dB, and 25.7 dBm, respectively. For DCS1800, the NF, gain, and output IP3 are 3.3 dB, 21.3 dB, and 22.5 dBm, respectively. The chips are biased at 3 V with a current consumption of 182 mA for the GSM900 receiver and 167 mA for the DCS1800 receiver.

TABLE I
$\mathrm{NF_{sys}}$ AND IIP3 REQUIREMENTS FOR GSM AND DCS BASE STATIONS

	GSM 900		DCS 1800	
	Micro	Normal	Micro	Normal
Sref (dBm)	-97	-104	-102	-104
NFsys (dB)	15	8	10	8
Interferer Pint (dBm)	-43	-43	-49	-49
IIP3 (dBm)	-10	-8	-18	-17
Pin-band (dBm)	-11	-13	-20	-25

II. GSM Receiver Requirements

System requirements have been derived from GSM 05.05 specification [1], and are summarized in Table I.

The details given are for micro and normal category of base stations. The most stringent reference sensitivity levels (S_{ref}) is required by the normal-type base station in each band. The micro base station, i.e., type "M3," has the most stringent in-band blocking requirement ($P_{\text{in-band}}$). In this case, the reference sensitivity must be maintained in the presence of a -11 dBm (GSM900) and -20 dBm (DCS1800) blocker at an offset frequency of 800 kHz or more. Reference [1] also specifies a co-channel interference (CI) ratio of 9 dB. Given that the temperature is 290 K and the GSM channel bandwidth B is 200 kHz, a maximum system NF ($\mathrm{NF_{sys}}$), referred to the input, can be derived using the minimum detectable signal (MDS), which is given in the following:

$$\mathrm{MDS} = S_{\mathrm{ref}} - C/I = -174\ \mathrm{dBm} + 10\log B + \mathrm{NF_{sys}}. \tag{1}$$

Values calculated using (1) for maximum $\mathrm{NF_{sys}}$ are given in Table I.

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For the intermodulation requirements, the reference sensitivity should be maintained when two tones of interference level $P_{\rm int}$, at 800- and 1600-kHz offset, shown in Table I, and a signal 3 dB above the reference sensitivity are input into the receiver [1]. In this case, to maintain a total $C/(I+N) = 9$ dB, the noise floor (N) and intermodulation level (I) should have a carrier-to-interference ratio of 12 dB. Therefore, the third-order intermodulation level (IMD3) is given by the following:

$$\text{IMD3} = P_{\rm int} - (S_{\rm ref} - 12 \text{ dB}) \tag{2}$$

and the minimum input referred intercept point (IIP3) is given by the following:

$$\text{IIP3} = P_{\rm int} + \text{IMD3}/2. \tag{3}$$

The calculated values of minimum IIP3 are given in Table I for the GSM900 and DCS1800 base stations. Reference [1, Sec. 6.1] requires that sensitivity of the receiver be maintained up to an input power level of -15 dBm for GSM900 and -23 dBm for DCS1800. To pass this test and the in-band blocker test, input power into the receiver chain of $P_{\text{in-band}}$, the gain of the receiver chain must not be compressed. If the gain is compressed, the channel CI ratio will degrade, reducing the sensitivity of the receiver and increasing the NF. Therefore, a receiver chain with an in-band 1-dB compression point, referred to as the input $P_{\text{in}(1\,\text{dB})}$, of greater than $P_{\text{in-band}}$, will meet the above tests.

To meet all base-station category specifications mentioned above, the receiver chain will have a target: NF of less than 8-dB in-band, IIP3 greater than -8 dBm (GSM900) and -17 dBm (DCS1800) and $P_{\text{in}(1\,\text{dB})}$ greater than -11 dBm (GSM900) and -20 dBm (DCS1800).

III. Receiver Architecture

A. Specification Partitioning

To meet demanding requirements detailed above, gain, NF, and linearity partitioning of the integrated receiver has to be done with great care. The whole receiver chain was considered in order to meet the GSM900 and DCS1800 targets given above. A single down-conversion receiver architecture was assumed for each GSM900 and DCS1800 receiver chain. Additional receiver requirements were that: 1) a loop test switch be included; 2) the chain could be used with an integrated low-noise amplifier (LNA) or with an external LNA; 3) an external 3-dB splitter is incorporated into the chain for a diversity channel; and 4) the chain could be used at various IFs, up to 300 MHz, and that channelization filters would be included to achieve a close to channel rejection of greater than 70 dBc [2]. It was assumed that the diversity output would occur before the mixer in the receiver chain.

The RF amplification is done in two stages to allow for the use of an external LNA. The gain of the first-stage LNA should be as low as possible while still maintaining good overall NF. The second-stage LNA should exhibit high linearity, while its NF is slightly less critical. The combined gain of the two LNAs should be limited so that the input compression requirements of the mixer are not stressed. Image filtering should be done before the mixer and after RF amplification so that image noise at IF is minimized and does not degrade the receiver chain NF. Noise is generated within the RF amplifier at the desired frequency and the image frequency. An external image filter is used so that different filter specifications, required for large and small IFs, could be accommodated.

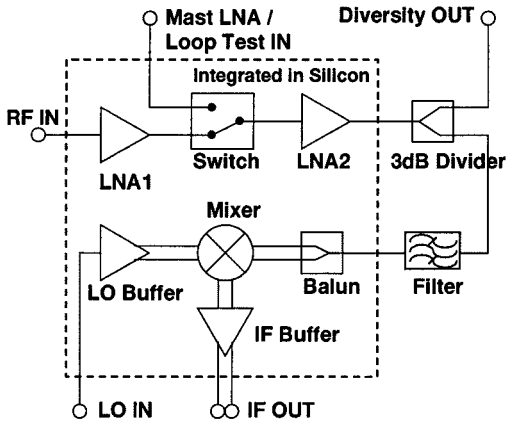

Fig. 1. Receiver chip block diagram.

The mixer should preferably be passive, to assure high linearity and low NF. The IF amplifier should follow the mixer and have sufficient gain to limit the effect of high insertion loss, channel filters (surface acoustic wave (SAW) devices) on the overall receiver chain NF. However, boosting the gain at the IF stage has less effect on overall linearity than if provided in front of the mixer. A high linearity and output power compression response is required of this amplifier, as this will degrade the linearity and $P_{in(1\,\text{dB})}$ of the chain if it is too low.

When designing the gain partitioning for the integrated receiver, great effort was made to maintain a high linearity for the chain, while minimizing NF and using parts with high input compression performance to accommodate the stringent blocking requirements given in [1].

The criterion discussed above dictate the radio architecture shown in Fig. 1. After specification partitioning, it is determined that the NF for both LNA stages should be 1.5–2 dB, and output IP3 of the second stage should be higher than 20 dBm. The combined gain of the two LNAs should be above 20 dB. The mixer IIP3 should be between 15–25 dBm, with the NF lower than 8 dB. Two channelization filters are required to achieve a rejection of 70 dBc. This implies, with current commercial parts, that the loss following the mixer will be in excess of 12 dB. The IF amplifier will require greater than 15-dB gain and IIP3 of greater than 15 dBm. The MDS level of any baseband or demodulation circuitry at the end of the receiver chain sets the lower limit on total receiver-chain gain. Total receiver-chain gain is assumed to be greater than 26 dB.

B. RFIC Implementation

The block diagram of GSM900/DCS1800 radio receivers [5] is shown in Fig. 1. Simplified schematics of the receiver chip are shown in Fig. 2.

The LNA before mixer is partitioned into LNA1 and LNA2. The input to LNA1 is connected to a duplexer. The switch between LNA1 and LNA2 is needed for loop test once the chip is mounted in the system. The second port of the switch can

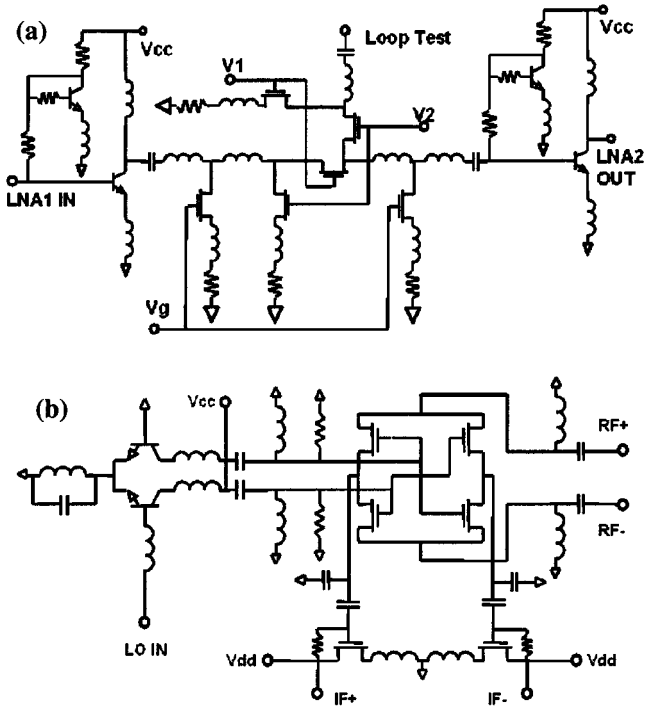

Fig. 2. Circuit schematic showing: (a) LNA1, switch, and LNA2 and (b) LO buffer amplifier, mixer, and IF buffer amplifier.

also be used as the input to the chip from an external mast-top LNA. The output of LNA2 is connected to a 3-dB power divider of which one output is used for diversity, while the other is connected back on-chip after a dielectric. The dielectric filter is used to reject image band noise and other out-of-band interference. The on-chip balun converts a single-ended input to a differential signal for the balanced mixer. The on-chip local oscillator (LO) buffer amplifier converts a single-ended LO input to a differential output and amplifies its power level to drive the double-balanced mixer. The IF port of the mixer is connected to the IF buffer before channel-select SAW filters or IF sampling.

The IF amplifier is placed directly after the mixer in order to minimize the effect of the channelization filters on the system NF.

All of the building blocks are integrated using Agere Systems' (formerly Lucent's Microelectronics) 0.25-μm silicon BiCMOS process, except the 3-dB power divider and dielectric filter. The silicon substrate has a resistivity of 10 $\Omega \cdot$ cm. The circuits were designed using Agilent ADS simulation software.[1] All of the RF inductors required in the circuits are integrated on-chip and have a Q value of approximately ten and inductance values ranging from 2.5 to 11 nH. Higher integrated inductor Q values can be achieved; however, they would employ a fabrication process with a thicker top metal (e.g., 5 μm), a copper top metal, or a higher resistivity substrate. These additional process features add cost to the fabricated chips and were not required in our design.

A thick top-level metal is used in the RF path through the chip to minimize series resistive losses and reduce capacitance to

[1]Circuit design simulation software, ADS ver. 1.3, Palo Alto, CA 94303.

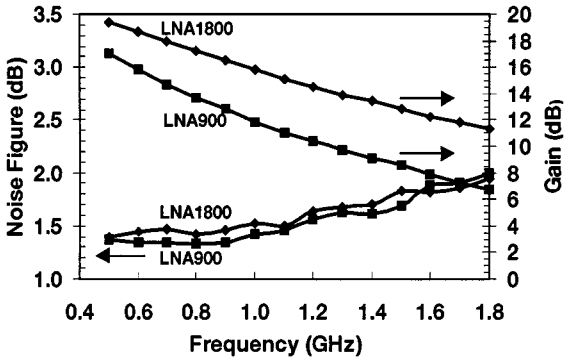

Fig. 3. Gain and NF response of 900- and 1800-MHz LNA.

substrate parasitic elements, which introduce unwanted loss into the signal path and degrade the Q of integrated spiral inductors.

IV. Receiver Functional Blocks

This section describes the detailed measured performance of the individual functional blocks in the receiver. These circuits were tested on-wafer, while integrated receivers were tested in packages on custom-design boards. In the integrated receivers, bipolar transistors are used for LNA1, LNA2, and LO buffer, whereas CMOS transistors are used for switch, mixer, and IF buffer. The bipolar transistor is chosen for its low-noise behavior (both 50-Ω NF and $1/f$ noise), whereas a CMOS transistor is needed for linearity, switching properties, and good isolation. All circuit blocks were designed to operate with a supply voltage of 3 V, where biasing is required.

A. LNAs

A single-stage common-emitter configuration was chosen for both LNAs in each band, in order to achieve high linearity and low NF [6]. Emitter sizes of 76.8 μm^2 at 900 MHz and 49.92 μm^2 at 1800 MHz were chosen to yield good NF, gain, and input voltage standing-wave ratio (VSWR) at the design frequency. On-chip impedance matching with inductors at the input was avoided since any extra loss at the input would increase the NF. Degeneration inductance was used in the emitter to improve input and output return losses and to increase IIP3. Although LNA1 and LNA2 were designed to have similar gain, in link budget partition, LNA1 was optimized for low NF, and LNA2 for high IIP3 [7]. The gain and NF response versus frequency for the two LNAs, in each band, is shown in Fig. 3.

In the GSM900 receiver, LNA1 has 1.4-dB NF, 13-dB gain, and 9.3-dBm IIP3, while LNA2 has 2.5-dB NF, 9.6-dB gain, and 17-dBm IIP3. In the DCS1800 receiver, LNA1 has 1.9-dB NF, 11.3-dB gain, and 3.7-dBm IIP3, while LNA2 has 2.1-dB NF, 12.2-dB gain, and 10.7-dB IIP3. A collector bias current of 13 and 11 mA was used for LNA1 in GSM900 and DCS1800 bands, respectively; 33 and 22 mA was used for LNA2 in GSM900 and DCS1800 bands, respectively.

B. SPDT Switch

This analog RF switch has a broad-band performance covering both GSM900 and DCS1800 bands and has no current

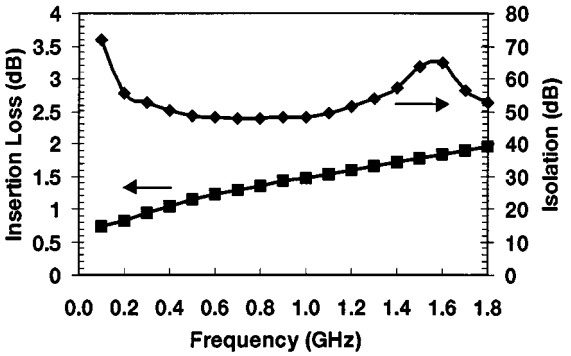

Fig. 4. NMOS switch isolation and insertion loss response with out dc blocking capacitors.

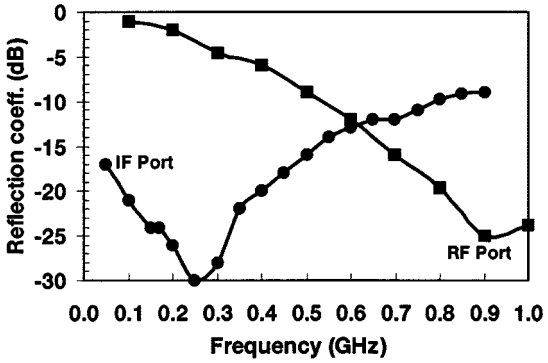

Fig. 5. Reflection coefficients at RF and IF ports for the 900-MHz mixer.

consumption. It consists of six NMOS transistors, each having a total gatewidth of 172.8 μm. The single-pole double-throw (SPDT) design has a similar topology to that shown in the GaAs MESFET switch design [8] and is matched to 50 Ω at each switch port. It exhibits 48-dB isolation at 900 MHz and 52-dB isolation at 1800 MHz. The insertion loss of the switch is 1.4 dB at 900 MHz and 2 dB at 1800 MHz, without dc blocking capacitors. The frequency response of isolation and insertion loss response is shown in Fig. 4.

In order to isolate LNA1 drain bias from LNA2 gate bias, a 30-pF dc blocking capacitor is included at each port of the switch. High isolation is achieved by using series inductors to achieve a good RF match to 50 Ω at each port and an NMOS device layout with very low parasitic capacitance. The insertion loss of the switch is dominated by the series resistive loss of the inductors and substrate parasitic shunt capacitance of dc blocking capacitors. With this parasitic capacitance, the insertion loss increases by 0.8 dB at 900 MHz and 1.3 dB at 1800 MHz. The IIP3 of the switch is 30 dBm at 900 MHz and 27 dBm at 1800 MHz.

C. Mixer

To achieve the best receiver NF and linearity simultaneously, a resistive CMOS mixer is used. This type of mixer has very high IIP3 compared with other mixer types [9]. Traditionally, such a mixer has been implemented using GaAs FET devices. However, a resistive mixer using a silicon MOSFET can achieve similar performance at a much lower cost. Both the 900- and 1800-MHz mixers are passive devices and, therefore, require no dc bias. These resistive CMOS mixers have a double-balanced ring structure and maintain their conversion loss level over a wide range of an LO input power level [10]. The conversion loss of the 900- and 1800-MHz mixer is 6.3 and 6.4 dB, respectively. The conversion loss varies by less than 0.5 dB for an LO input power ranging from 8 to 18 dBm. This feature enables overall receive path gain to be insensitive to LO buffer output power. A very high IIP3 of 19.7 and 21.9 dBm is achieved at 900 and 1800 MHz, respectively, with a LO input power of 13 dBm.

The NMOS device size used for both circuits was chosen to yield high IIP3 (requiring large size) and a balanced IF output impedance of 100 Ω. This impedance requirement removes the need to integrate large-value IF impedance matching components on-chip. In order to reduce conversion loss and in-band ripple, caused by reflection from impedance mismatch with the external image reject filter and IF filters, it is important to achieve good impedance matching at the input and output ports. The 1800-MHz mixer achieves an RF reflection coefficient of -19 dB at 1800 MHz and an IF reflection coefficient of less than -16 dB over a 500-MHz bandwidth. The RF and IF port reflection coefficients of the 900-MHz mixer are shown in Fig. 5.

In order to minimize parasitic series resistance within the device and to enable it to handle large ac signals, the gate, drain, and source fingers are all individually connected to thick wide metal feeds. This is particularly critical at the gate since it is driven by a large LO signal. The balanced RF port input impedance is matched to 100 Ω with shunt spiral inductors, which also act as high-pass filter elements, increasing the IF to RF isolation. The RF–IF isolation is 40 dB for the 900-MHz mixer and 54 dB for the 1800-MHz mixer. High LO–RF and LO–IF isolation of better than 54 and 50 dB, respectively, were achieved by minimizing the parasitic capacitance in each NMOS device to below 25 fF by employing grounded guard rings and by utilizing a strongly symmetrical mixer layout.

D. LO Buffer Amplifier

Since the resistive mixer requires a high LO drive, a linear buffer amplifier at the LO port is integrated on-chip. The LO buffer also functions as an active balun that converts a single-ended LO signal to a differential LO signal. High-output $P_{1\,\mathrm{dB}}$ is required to drive the resistive mixer in order for it to achieve high IIP3. This criterion is met by the buffer amplifier, which has an output $P_{1\,\mathrm{dB}}$ of greater than 13 dBm. A narrow-band gain response is also a desired feature for the LO buffer amplifier. This will reduce the level of LO harmonics entering the mixer and thereby reduce the level of higher order intermodulation products, which may block the wanted signal. At the output $P_{1\,\mathrm{dB}}$ power level, this amplifier exhibits 25- and 43-dBc suppression of the second and third harmonics, respectively. To maintain the LO signal purity and meet the GSM blocking test requirement, the LO buffer should have low residual phase-noise performance. This type of noise adds to the oscillator phase noise entering the mixer and, therefore, should be as low as possible. A measured residual phase noise of less than -155 dBc/Hz at offset frequencies of 100 kHz was achieved [11]. This measurement was made at a frequency of 1.6 GHz.

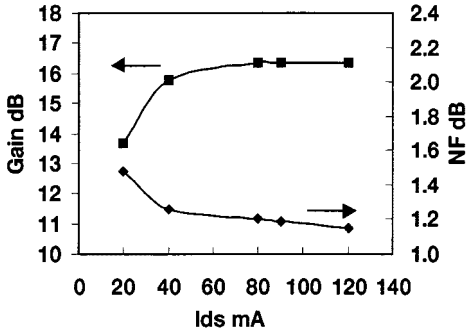

Fig. 6. Gain and NF variation with drain–source current for a single NMOS IF amplifier biased at 3 V. For the receiver chain, each IF amplifier is biased at 45 mA.

The amplifier gain is greater than 8 dB from 800 MHz to 1.6 GHz. The amplitude balance error is better than 1 dB and the phase balance error is less than 2°. The circuit is operated at 45 mA, with a single supply voltage of 3 V.

E. IF Buffer Amplifier Block

An IF buffer amplifier is connected after the mixer to compensate for the conversion loss of the mixer, image filter, and 3-dB splitter and to reduce the effect of the channelization filter loss on the receiver NF. A very high IP3 is required for the IF buffer so that this stage does not limit the linearity or cause gain compression of the receiver chain.

The amplifier block consists of two separate single-ended common-source amplifiers, one for each IF output from the mixer. The two IF amplifier outputs are connected to an external balanced SAW filter.

A very large NMOS device is used within this amplifier to provide low NF and high IIP3. The total gatewidth of this device is 3120 μm and is arranged in a simple common-source resistive feedback configuration. This stabilizes the device while reducing lower frequency gain and achieving low-port reflection loss. A 4.6-nH spiral inductor between source and ground is used to increase linearity and optimize input and output impedance. Gain greater than 13 dB and NF of less than 1.6 dB was obtained from near dc to 300 MHz. Fig. 6 shows the gain and NF variation of the NMOS IF amplifier with an $I_{\rm ds}$ level at a mid-band IF.

It is important for the IF amplifier to have a design that has some tolerance to changes in device bias current. This is more important with very large NMOS devices because small changes in the fabrication process could lead to large changes in gain. This could result in a reduction in the amplifier and receiver chain linearity. Fig. 6 illustrates that the amplifier gain is insensitive to bias above an $I_{\rm ds}$ level of 40 mA. Within the receiver chain, the two IF amplifiers are each biased at 45 mA from a 3-V supply. This bias current was chosen in order to minimize the receiver power dissipation while retaining some degree of bias stability.

The IF buffer amplifier block achieves 1.2-dB NF, 16.3-dB gain, and 18.5-dBm IIP3 with bias of 90 mA and 3 V. With a reduced bias current of 40 mA, the IF buffer amplifier block achieves 1.3-dB NF, 15.8-dB gain, and 13.1-dBm IIP3. The output $\rm P_{1\ dB}$ for 40 and 90 mA is 17.8 and 23.8 dBm, respectively. As a comparison, the IF amplifier employed within [2] referred to as the "inter-SAW amplifier" was fabricated on a high-speed silicon bipolar process and used a bias of 80 mA from a 5-V supply. This amplifier has a gain of 15 dB, NF of 5 dB, and output $\rm P_{1\ dB}$ is 17 dBm.

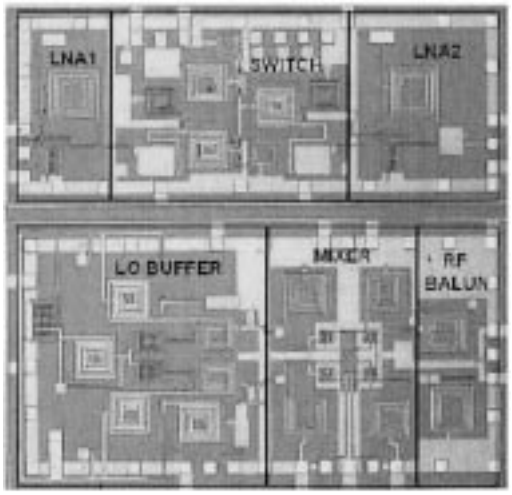

Fig. 7. DCS1800 receiver RFIC.

The input port is matched to balanced 100-Ω impedance and the output port is matched to balanced 200-Ω impedance. Measurements at each port showed a reflection coefficient of better than -10 dB from near dc to 300 MHz. The output impedance of 200 Ω was chosen to impedance match the input of subsequent IF channelization filters.

V. Integrated Receiver

The chip layout is designed to fit into a TQFP-48 package with a 7 mm $\times$ 7 mm body size. Both chips have a similar size of about 3.5 mm $\times$ 3.5 mm. To reduce the ground inductance and improve the performance, the ExposedPad TQFP-48 package is used [12]. The package has a backside ground pad that provides a very good RF ground to the chip. With a number of ground bond wires directly bonded to the common ground pad, the total ground inductance is reduced to below 0.5 nH. Since the chip size is limited in this package, the CMOS IF buffer amplifier block is packaged separately. This also allows the reuse of IF amplifiers after channel-selection SAW filters to optimize overall system gain and sensitivity.

The die photo of a DCS1800 integrated chip including LNA1, switch, LNA2, mixer, RF balun, and LO buffer is shown in Fig. 7. The GSM900 integrated chip is similar in layout.

Chips were tested on the custom circuit boards, built on a Rogers RO-4003 substrate with a dielectric constant of 3.38 and a thickness of 0.5 mm. SMA connectors were used for RF, LO, and IF ports (Fig. 8). The signals were routed to the SMA connectors via 50-Ω lines, which were 1.1-mm wide on this material. The board dimensions were 50 mm $\times$ 50 mm.

The LNA1, switch, and LNA2 chain NF, gain, and linearity were evaluated over the whole GSM900 and DCS1800 bands. IIP3 was measured using two continuous wave (CW) signals at the input of LNA1, at 800 and 1600 kHz away from the carrier, and an HP8563E spectrum analyzer was used at the LNA2

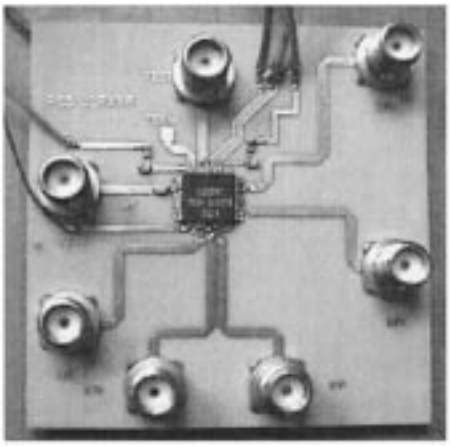

Fig. 8. Circuit board used to test packaged DCS1800 receiver RFIC.

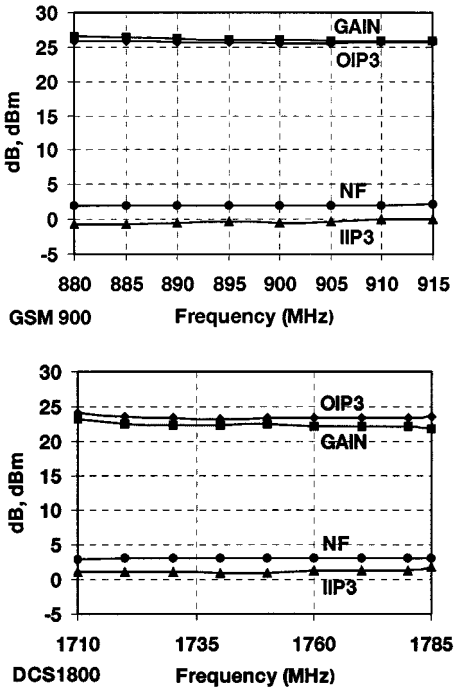

Fig. 9. Frequency response of GSM900 and DCS1800 receiver RFICs from LNA1 input to IF amplifier block output.

output to determine intermodulation levels. NF and gain of this chain were measured using an HP8970B NF meter, with the NH8971C test set and HP346A noise source. The IF amplifier was tested in the same manner as the LNA chain. An LO buffer/mixer was tested separately by applying a test signal at LO and RF ports. Receiver NF, gain, and IIP3 were calculated in Syscal[2] using measured data for the amplifier chain, mixer, balun, and IF amplifier, and assuming a loss of 4.7 dB for the cascaded 3-dB splitter and image reject filter.

The frequency responses of both receivers are shown in Fig. 9.

The integrated receivers achieve better than 2.1-dB NF, 25.8-dB gain, −0.1-dBm IIP3 in the GSM900 band, and better than 3.3-dB NF, 21.3-dB gain, and 1.21-dBm IIP3 in the DCS1800 band. The isolation between the two RF input

[2]System simulation software, Syscalc ver. 4.06.00, Arden Technol. Inc., Forest, VA 24551.

TABLE II
INTEGRATED GSM900 RECEIVER PERFORMANCE

GSM900 receiver	NF (dB)	Gain (dB)	P_{1dB} (dBm)	IIP3 (dBm)	OIP3 (dBm)	I_{DC} (mA)
LNA1	1.4	13.0	-5.5	9.3	22.3	12.9
LNA2	2.5	9.6	3.0	17.0	26.0	32.9
Broad band switch	2.2	-2.2	17.5	30.0	27.8	0
Mixer w/ LO buffer	6.3	-6.3	10.3	19.7	12.6	45.8
IF buffer	1.2	16.3	7.5	18.5	34.8	90
Integrated Receiver	2.1	25.8	-7.8	-0.1	25.7	182

TABLE III
INTEGRATED DCS1800 RECEIVER PERFORMANCE

DCS1800 receiver	NF (dB)	Gain (dB)	P_{1dB} (dBm)	IIP3 (dBm)	OIP3 (dBm)	I_{DC} (mA)
LNA1	1.9	11.3	-9.0	3.7	15.0	10.7
LNA2	2.1	12.2	-3.0	10.7	22.9	22.1
Broad band switch	3.3	-3.3	18.5	27.0	23.7	0
Mixer w/ LO buffer	6.4	-6.4	11.3	21.9	15.5	44.6
IF buffer	1.2	16.3	7.5	18.5	34.8	90
Integrated Receiver	3.3	21.3	-7.9	1.2	22.5	167

paths on the chip is better than 48 dB in both bands. The chips are biased at 3 V with a current consumption of 182 mA for the GSM900 receiver and 167 mA for the DCS1800 receiver. While this power consumption might seem high compared to handset chips, it is actually significantly lower than for other base-station RF front-end solutions. Reference [2] has GaAs RXIC1 (mixer, LO buffer, IF amp) and an "inter-SAW amp" consuming 290 mA from a ±5-V supply. The chips within this paper can be used at a lower bias current with the tradeoff in linearity, which would be adequate for applications with more relaxed specifications, such as for handsets and an indoor local area network (LAN). A summary of the integrated receivers performance and individual function performance is shown in Tables II and III.

VI. EMBEDDED GSM900/DCS1800 RECEIVER PERFORMANCE

In order to demonstrate how the integrated receiver may be used within a GSM900 or DCS1800 base-station receiver chain, an example chain is proposed. This allows a more realistic view of the possible overall receiver characteristics to be reached.

Fig. 10 shows the example receiver chain using the integrated receiver and two additional IF amplifier blocks, as described in this paper. The two IF filters could be used as channelization filters or antialiasing filters. The insertion loss shown for the duplexer and filters is for in-channel performance. The demodulator/baseband circuitry is represented by a single passive block with a NF of 30 dB and high IIP3.

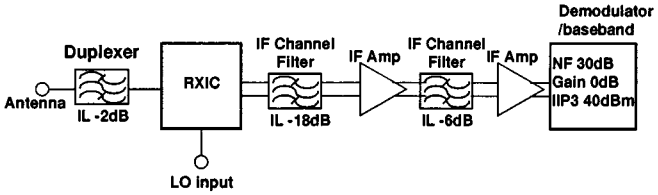

Fig. 10. Example receiver chain using receiver RFIC (RXIC) and IF buffer amplifier block (IF AMP).

TABLE IV
RECEIVER CHAIN PERFORMANCE

	NFsys	IIP3	Pin(1dB)	Ssys
GSM900	5.5 dB	-1.7dBm	-10 dBm	-107 dBm
DCS1800	7.8 dB	1.1 dBm	-8 dBm	-105 dBm

The RF performance and system sensitivity $S_{\rm sys}$ achieved in each band of the receiver chains is shown in Table IV. The receiver chains also achieved 32.4-dB gain at GSM900 and 27.9-dB gain at DCS1800. By comparing the system sensitivity achieved with the reference sensitivity given in Table I, it can be seen that this chain meets this requirement in each band. Comparisons of a system NF and linearity also show compliance with the specifications. As the in-channel input $\rm P_{1\,dB}$ is higher than that required for the adjacent channel blockers, across the whole GSM900 or DCS1800 band, the receiver chain will meet the blocker requirement on input compression. The performance of the example receiver chain shows that the integrated receivers, presented in this paper, can be used to achieve GSM900 and DCS1800, normal and micro base-station performance.

VII. CONCLUSIONS

The integrated RF receivers that have been presented in this paper meet GSM900 and DCS1800 normal and micro base-station specifications in a low-cost silicon technology. This also demonstrates the feasibility of making compact and low-cost receiver units for base-station applications and is essential to the hardware implementation of SDMA or similar technologies that use multiple radios for space and time signal processing to increase capacity in future wireless communication systems.

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